(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 434 138 A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90203302.6

(22) Date of filing: 13.12.90

(51) Int. Cl.5: H01L 23/532, H01L 21/90, H01L 21/268

(30) Priority: 18.12.89 US 452860

(43) Date of publication of application: 26.06.91 Bulletin 91/26

(84) Designated Contracting States: DE FR GB IT NL

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(54) Method of forming an aluminum conductor with highly oriented grain structure.

(57) A method for reducing electromigration of aluminum or aluminum alloy polycrystalline conductors on a dielectric layer of a semiconductor device in which an array of columns holes at least three hole wide in said dielectric layer is etched, said holes extending only partially through said layer in a line pattern corresponding to that of a desiring interconnection pattern, the pitch of said holes being about 1/2 - 5 μm and said holes having a depth of 1/10 - 1/2 μm. Then a thin film of aluminum or aluminum alloy is deposited having a thickness at least sufficient to fill said holes on the surface of said dielectric layer provided with said holes. Said film of aluminum or aluminum alloy is scanned with a laser beam of an intensity sufficient to melt said film and cause it to flow and be planarized and upon cooling forming an oriented crystal structure with grain boundaries aligned orthogonally to rows and columns of the hole pattern. A photoresist mask is aligned with said crystal structure in a manner such that crystal boundaries extend substantially only in a direction across the width of the desired conductor lines and aluminum material is removed from said crystal structure outside of said desired conductor lines by plasma etching said crystal structure thorough said aligned photoresist mask.

FIG. 2

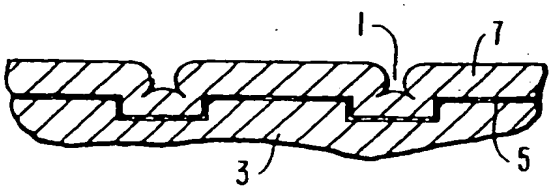

FIG. 4

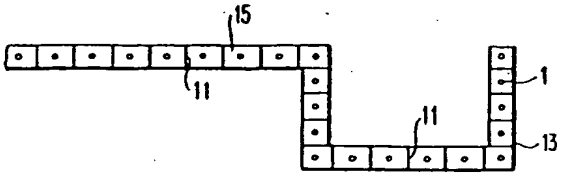

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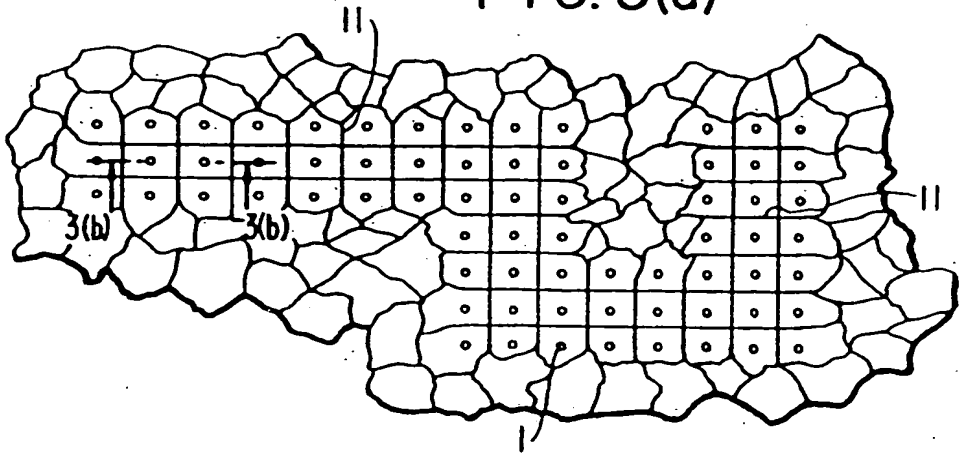
FIG. 3(a)



METHOD OF FORMING AN ALUMINUM CONDUCTOR WITH HIGHLY ORIENTED GRAIN STRUCTURE.

The invention in this case relates to a method of reducing the electromigration of aluminum or aluminum alloy conductors in semiconductor devices.

A frequent cause of failure in aluminum or aluminum alloy conductors employed in high density integrated circuits is found to be electromigration. Electromigration occurs particularly under the conditions of high DC current and high temperature conditions, which conditions occur very frequently in the operation of semiconductor devices. Under these conditions, aluminum metal is transported by the current passing through the aluminum containing conductors, thereby causing the aluminum to form undesired voids and undesired excess deposits. As a result, undesired resistance in these devices is increased to such an extent that an excess amount of electrical and/or heating resistance results, leading to premature failure of such devices.

It is known that electromigration in polycrystalline aluminum conductors essentially proceeds along grain boundaries. These grain boundaries, which are disordered regions between polycrystalline grains, have a lower activation energy for diffusion than that of the bulk of the crystalline grain <111>.

Based on this information, a method is described in Pierce, U.S. Patent 4,352,239 in which electromigration is significantly suppressed by a method insuring that the grain boundaries do not extend along the length of a conducting line, but rather extend directly across it.

In this method the grains of the film are formed to be at least as long as the width of the conducting lines and comparable to the length of these lines. As taught by the Pierce patent, unless the average grain size is in fact comparable to the conductor width, there is a high probability of a grain boundary extending for a sufficient distance along the length of the conducting line for electromigration to occur and resulting in failure of the semiconductor device.

Electromigration of aluminum polycrystalline conductors in semiconductor devices is significantly reduced by the method of the Pierce patent. This is achieved by forming the conductors under conditions such that the average grain size grows larger than the width of the conductors and then heat treating the conductors. As a result, grain boundaries are formed which tend to orient themselves across the conductors while the growth of grain boundaries extending along the length of the conductors is virtually stopped.

The resultant orientation of the grain boundaries which is commonly called a "bamboo" structure is found to significantly suppress electromigration in aluminum alloy polycrystalline conductors.

The van de Ven et al U.S. Patent 4,566,177 also shows a method of significantly increasing the electromigration resistance of aluminum alloy conductors in semiconductor devices by the formation of a "bamboo" structure. According to the method of this patent, such a structure is formed by rapidly heating and cooling the conductors, specifically subjecting the conductors to a heat-cool cycle with a peak temperature of 520 - 580° C and as a minimum temperature, ambient temperature, and with a cycle time of about 5 to 30 seconds. The van de Ven patent shows that such cycles may be readily achieved with the use of high intensity CW visual light lamps.

It is the object of this invention to provide a novel method for the reduction of electromigration of aluminum and aluminum alloy polycrystalline conductors in semiconductor devices.

According to the method of the invention, electromigration of aluminum and aluminum alloy polycrystalline conductors is found to be significantly reduced by a method characterized by the following procedure:

a) first, an array of columns of holes of at least three hole wide rows is etched in a dielectric layer extending only partially through the layer in rows and columns and arranged in a line pattern corresponding to that of a desired interconnection pattern, the holes are positioned relatively close to each other, with the pitch being about 1/2 - 5 µm and the depths of the holes being about 1/10 to 1/2 µm,

b) a thin film of aluminum or aluminum alloy of a thickness sufficient to at least fill the holes is then deposited on the surface of the dielectric layer provided with these holes,

c) the film of aluminum or aluminum alloy is then scanned with a laser beam of an intensity sufficient to melt the film and cause it to flow and to planarize and upon cooling, the film forms an oriented crystal structure with the grain boundaries aligned orthogonally to the rows and columns of the hole pattern,

d) a photoresist mask is then aligned with the resultant grain structure in a manner such that the grain boundaries extend substantially only in a direction across the width of the desired conductor lines and

e) the crystal structure outside of the desired conductor lines is then removed by plasma etching through the aligned photoresist mask.

The invention further will be explained with

reference to a drawing in which:

Fig. 1 is a top view of an array of holes provided in a dielectric layer according to one step of the method of the invention,

Fig. 2 is a cross-sectional view of the array of holes of Fig. 1 provided with a thin TiW layer and an Al film according to an additional step of the method of the invention,

Fig. 3(a) is a top view of the aluminum film after melting by laser scanning and recrystallization showing the resultant oriented crystal structure of the aluminum film provided with grain boundaries aligned orthogonally to the rows and columns of the holes,

Fig. 3(b) is a cross-sectional view of the oriented crystal structure shown in Fig. 3(a) and

Fig. 4 is a top view of a conductor produced by the plasma etching of the oriented polycrystalline aluminum structure of Fig. 3(a) through the photoresist mask aligned with orthogonally aligned grain boundaries.

While good results have been achieved with a hole pitch of 1/2 - 5 μm, it has been found that a hole pitch of 2 - 4 μm is particularly useful. In any case, however, the hole pitch should be slightly greater than the desired Al conductor linewidth. The holes are etched so as to extend only partially into the dielectric layer. Particularly good results are achieved with hole depths of 1/10 - 1/2 μm.

While the aluminum or aluminum alloy film should be at least thick enough to fill the holes, this thickness preferably should be somewhat greater, for example from 1/2 - 2 μm. These films may be deposited by any well known means such as sputtering or evaporation.

The hole diameters should be less than the desired conductor linewidth, diameters of about 1/2 - 1 μm being particularly useful.

The dielectric layer may be a layer supported by one or more underlying layers or substrates or may itself be a self-supporting substrate.

The dielectric layer is generally formed of silicon dioxide. However, silicon nitride may also be employed.

In order to improve the flow of the aluminum material during laser scanning, a thin film, on the order of several hundred Å of an inorganic material such as TiW may be deposited on the dielectric layer before deposition of the aluminum film.

To assist in the melting and planarizing of the aluminum layer, the dielectric layer may be heated to an elevated temperature (for example of about 200 - 400 °C) while the aluminum film is being irradiated.

For a more complete understanding the invention will now be described in greater detail with reference to the figures of the drawing.

As shown in Fig. 1, an array of shallow holes 1 are etched into a planar layer 3 of silicon dioxide of a thickness of ~1.0 μm by plasma etching.

The holes, which are approximately 0.1 - 0.3 μm deep, have diameters of approximately 1μm are etched in 3 columns across at a pitch of 2 - 4 μm in a line pattern identical with a desired Al interconnect mask.

Then, as shown in Fig. 2, a thin layer of TiW 5 of in the order of about 200 - 1000 Å is provided by sputtering or physical vapor deposition on the silicon dioxide layer 3 and in the holes 1.

A thin film of Al 7 of a thickness of 0.5 - 1.5 μm is then deposited on the thin layer of TiW.

The film of Al 7 is then scanned with a laser pulse possessing sufficient energy to melt the Al material while the layer of silicon dioxide 3 is heated to 300 °C. As a result, the Al film 7 is caused to melt and flow and become planarized while recrystallized grain growth is propagated from the holes, the grain growth from adjacent holes converging, with an oriented structure being formed with grain boundaries 11 aligned orthogonally to the rows and columns of the array of holes 1 as shown in Figs. 3(a) and 3(b).

A photoresist mask (not shown) corresponding to the desired Al interconnected network is then aligned with the grain boundaries and undesired Al is then removed by plasma etching. The resultant Al conductors 13, a top view of which is shown in Fig. 4, consist of oriented grains 15 having boundaries 11 aligned perpendicular to its length.

Claims

1. A method for reducing electromigration of aluminum or aluminum alloy polycrystalline conductors on a dielectric layer of a semiconductor device characterized by the following procedure:

   a) etching an array of columns holes at least three hole wide in said dielectric layer, said holes extending only partially through said layer in a line pattern corresponding to that of a desiring interconnection pattern, the pitch of said holes being about 1/2 - 5 μm and said holes having a depth of 1/10 - 1/2 μm

   b) depositing a thin film of aluminum or aluminum alloy, a thickness at least sufficient to fill said holes on the surface of said dielectric layer provided with said holes,

   c) scanning said film of aluminum or aluminum alloy with a laser beam of an intensity sufficient to melt said film and cause it to flow and be planarized and upon cooling forming an oriented crystal structure with grain boundaries aligned orthogonally to rows and columns of the hole pattern,

d) aligning a photoresist mask with said crystal structure in a manner such that crystal boundaries extend substantially only in a direction across the width of the desired conductor lines, and

e) then removing aluminum material from said crystal structure outside of said desired conductor lines by plasma etching said crystal structure thorough said aligned photoresist mask.

2. The method of Claim 1 characterized in that the dielectric layer is heated to a temperature of 260 - 400 ° C while said layer of aluminum or aluminum alloy is scanned with the laser beam.

3. The method of Claim 1 characterized in that the holes are about 0.1 - 0.3 µm deep.

4. The method of Claim 2 characterized in that the holes are about 0.1 - 0.3 µm deep.

5. The method of Claim 1 characterized in that prior to the deposition of the aluminum or aluminum alloy a thin film of a flow improving material is deposited on the dielectric layer.

FIG. 1

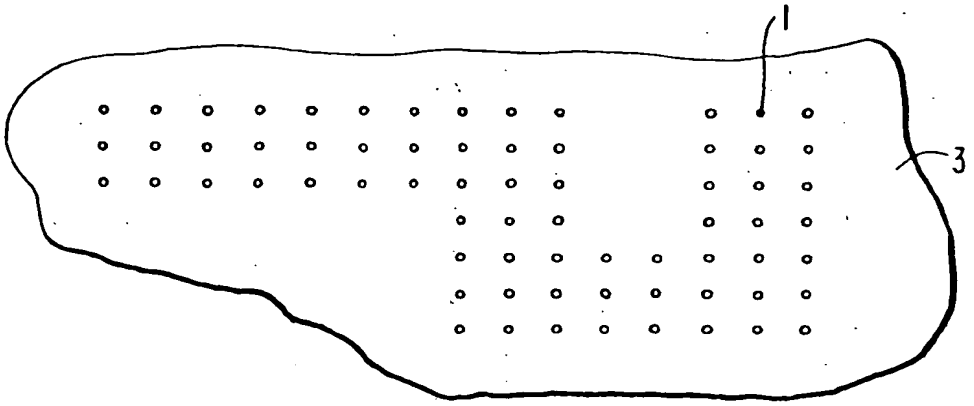


FIG. 2

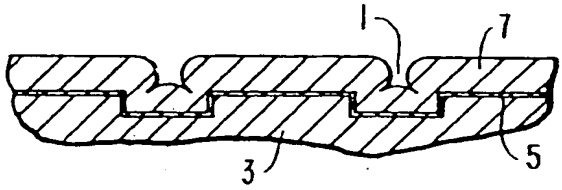


FIG. 3(a)

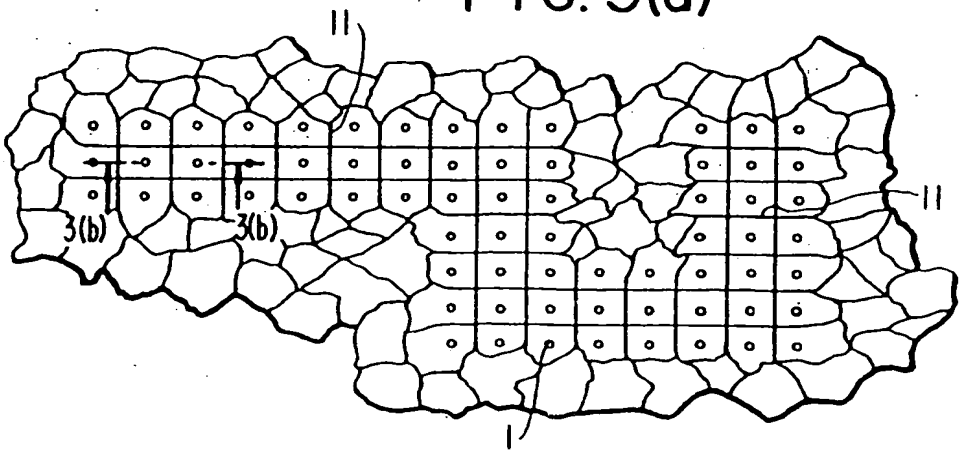


FIG. 3(b)

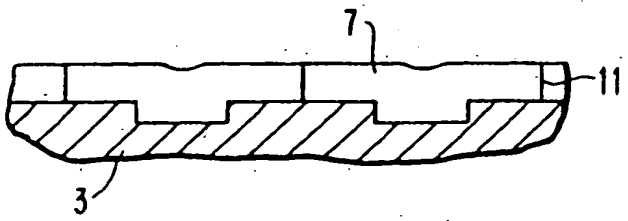
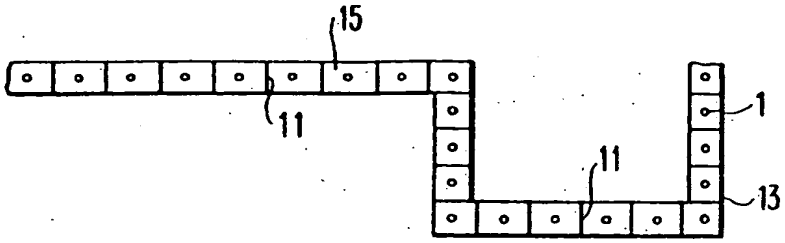


FIG. 4



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EUROPEAN SEARCH REPORT

Application Number

EP 90 20 3302

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
D,Y	US-A-4 352 239 (JOHN M. PIERCE) * column 2, line 18 - column 44; figures 2-4 * * column 3, line 3 - column 4, line 7 *	1-5	H 01 L 23/532 H 01 L 21/90 H 01 L 21/268
Y	US-A-4 758 533 (THOMAS J. MAGEE ET AL.) * column 6, lines 30 - 49 * * column 8, line 46 - column 9, line 34; claims 1, 4, 5; figures 6A-7 *	1-5	
A	EP-A-0 020 134 (M.I.T.) * page 5, line 1 - page 7, line 12; claims 1, 4; figures 1-7 *	1-5	
A	WO-A-8 101 629 (WESTERN ELECTRIC COMPANY INC.) * page 2, lines 10 - 27 * * page 3, line 29 - page 5, line 3; figures 3, 4, 9 *	1	
D,A	US-A-4 566 177 (EVERHARDUS P.G.T. VAN DE VEN ET AL.) * column 2, lines 18 - 48; claims 1, 4, 8; figures 2, 3 *	1	
A	Proceedings of the 2nd int. IEEE VLSI Multilevel Interconnection Conference 25 June 1985, SANTA CLARA, CALIFORNIA pages 24 -31; David B. TUCKERMAN et al.: "Pulsed laser planarisation of metal films for multilevel interconnects" * abstract * * pages 27 - 30 *	1,3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L
C 30 B

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
Berlin	05 March 91	KLOPFENSTEIN P R

CATEGORY OF CITED DOCUMENTS

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